Oxide Double-Layer Nanocrossbar for Ultrahigh-Density Bipolar Resistive Memory

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The semiconductor industry has long searched for promising methods to overcome the fundamental scaling limits of charge-based information storage devices. One of such methods is to increase integration density, which can be realized in the crossbar architecture.[1] As displayed in **Figure 1**a, the crossbar structure is composed of a set of parallel bottom electrodes, called bit-lines, and perpendicular top electrodes, called word-lines. The word- and bit-lines sandwich the memory device between them. Then the smallest possible cell size will be $4F^2$ (F = minimum feature size), where the distance between the electrodes is equal to the device size.[2,3] Note that this value of $4F^2$ is the highest integration density, which can be attainable with the 2D planar architecture.

However, due to its simplicity, the crossbar structure leads to a problem in reading the correct information in a designated cell (i.e., cell #1 in this figure), called the sneak path problem. As displayed with the yellow line in Figure 1a, the low resistive ON states of the undesignated neighboring cells may generate a sneak path in the crossbar array with applied external voltage between the word-line and the bit-line. This sneak path problem can be overcome by introducing additional switching elements between the memory elements and the electrodes. As shown in Figure 1b, the switching elements can block the leakage currents in the undesignated cells to facilitate the correct reading of the information in the designated cell. In the conventional charge-based memory technologies, Si-based transistors can be used as the switching elements. Unfortunately, the Si-based transistor itself occupies a 6–8F^2 space,[1,2] so this active device is not compatible with integration densities of $4F^2$. To overcome this obstacle, a new type of memory device must be developed without Si-based transistors, but still using the desirable crossbar architecture.

Recently, several groups proposed hybrid devices that combine a resistive memory element with a switching element in the crossbar architecture.[4–9] The resistive memory element facilitates resistance switching phenomenon, where the memory device can be switched between the bistable states, i.e., high resistance (OFF) and low resistance (ON) states, by an applied external voltage.[10–14] Since the resistance switching material can be operated with a simple metal–insulator–metal structure, it can easily be integrated in the crossbar architecture. However, proper selection of the resistive memory and switching materials remains to be an important issue. In addition, experimental evidence of how far we can reduce the size of such hybrid devices is still lacking.

Selection of the resistance switching material is particularly important. According to the recent review article by Waser et al.,[15] resistance switching can be classified depending on the origin and electric polarity required for switching: unipolar thermochemical memory,[16,17] bipolar electrochemical metallization,[18,19] and bipolar valence change memory effects.[20,21] Compared to the bipolar valence change memory effect, the former two effects are known to have significant obstacles for the realization of high-density memory device in terms of scalability and stability in switching parameters.[10,13,15,22] For example, memory elements based on unipolar resistance switching usually require high operating currents for the thermochemical process and show large fluctuations in their operational parameters.[23,24] Therefore, the bipolar valence change memory effect seems to have greater potential in terms of scalability and stability.[13,22] However, up to this point, there is no report on hybrid passive devices that use the bipolar valence change memory effect.

Here, we introduce a simple double-layer nanocrossbar device, which is composed of a valence change type bipolar resistive memory (BR) and a bidirectional switch (S) for high-density memory. To explore such a nanodevice, we fabricated TiO_2/VO_2 double layer, which exhibits 1BR and 1S functions, respectively. Note that TiO_2 resistance switching is known for its bipolar valence change memory effects.[13,21,25] In addition, VO_2 is a well-known threshold switching material, which can function as a bidirectional switch.[3,16,26] To explore the performance of the 1S-1BR device, we fabricated a 2×2 nanocrossbar array and verified the absence of the sneak path problem in the structure. To gain further insight into how far we can reduce the size of the 1S-1BR device, we measured local current–voltage (I–V)

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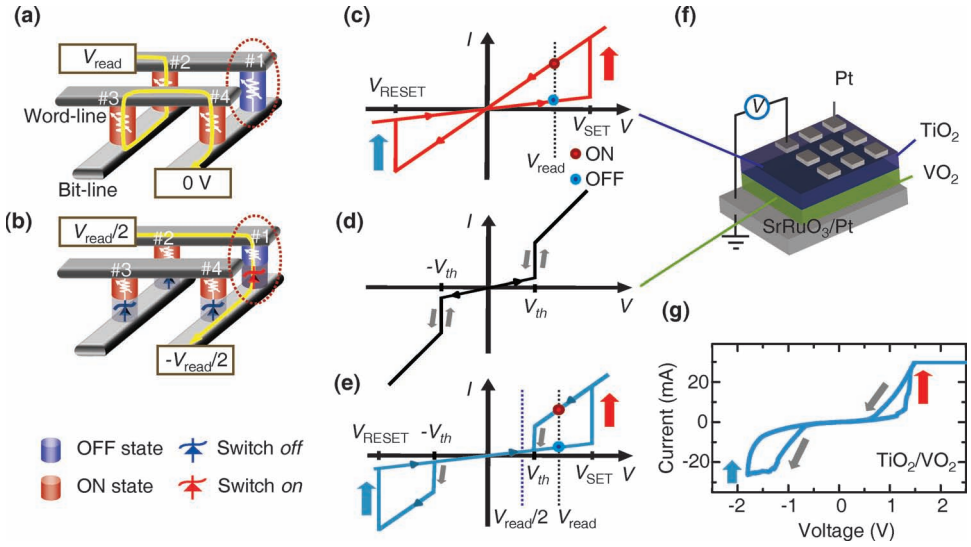

Figure 1. Necessity and operation principles of the one bidirectional switch-one bipolar resistive memory (1S-1BR) device structure. a) The occurrence of the sneak path problem, highlighted with a yellow line, in the 1BR device (ON: low resistance state (red) and OFF: high resistance state (blue)). b) A schematic of the 1S-1BR device, which overcomes the sneak path problem through the use of an additional switching element. Applying $V_{read}/2$ and $-V_{read}/2$ at the word- and bit-lines, respectively, the designated cell (#1) can be turned on without affecting the neighboring cells. c,d) Schematic diagrams of current–voltage (I–V) curves for the c) 1BR and d) 1S elements. V_{SET} and V_{RESET} are the set and reset voltages for the 1BR element. V_{th} is the switching-on (off) voltage for the 1S element. e) The I–V curve for the proposed 1S-1BR device implemented with the 1S and 1BR elements in series. When $V_{read}/2 < V_{th} < V_{read}$, the sneak path problem does not occur. f,g) Schematic diagrams of the TiO_2/VO_2 double layer for f) the 1S-1BR device and g) its experimentally measured I–V curve, which demonstrates that the 1S-1BR device functions as proposed.

curves of TiO_2/VO_2 double layer using an atomic force microscopy (AFM) conducting tip as a top electrode. The results suggest that ultrahigh densities exceeding 1 Tb in.$^{-2}$ are achievable with the 2D nanocrossbar array layout.

Figure 1c–f illustrates the principles of operation of the 1S-1BR device. As shown in Figure 1c, the 1BR element exhibits bistable states with high and low resistances, which function as the OFF and ON states of the memory, respectively. The OFF state can be changed to the ON state by applying a positive voltage called the set voltage (V_{SET}). Likewise, a change from the ON state to the OFF state requires a negative voltage called the reset voltage (V_{RESET}). As shown in Figure 1d, the 1S element can exhibit two volatile resistance states depending on the magnitude of the applied voltage. When the magnitude of the applied voltage is larger than the threshold voltage V_{th}, 1S attains the *on* state, which is different from the ON state for 1BR. When it is smaller than V_{th}, 1S attains the *off* state. Although the VO_2 film exhibits hysteretic behavior due to the nature of the first-order phase transition,[26] it is not essential for the operation of 1S-1BR. In the 1S-1BR device, the 1BR element must be connected to the 1S element in series, as displayed in Figure 1f. If this condition is satisfied, then the resulting I–V curve is shown in Figure 1e. When the read voltage, V_{read}, is applied, the state of the 1BR element can be read, i.e., the ON/OFF state of the 1BR element can be determined. On the other hand, when $V_{read}/2$ is applied, 1S must always be in the *off* state, which blocks the current flow through the 1S-1BR device. This operation can solve the sneak path problem. For the proper functioning of the 1S-1BR device, the following conditions must be satisfied: $V_{th} < |V_{RESET}|$ and $V_{th} < V_{SET}$. To prevent the sneak path problem, the resistance of the *off* state in 1S, R(1S, *off*), must be much greater than the resistance of the ON state in 1BR, R(1BR, ON), and R(1BR, OFF) + R(1S, *on*) < 2 × [R(1BR, ON) + R(1S, *off*)], as shown in Figure 1b.

To test the feasibility of a 1S-1BR device, we fabricated a TiO_2/VO_2 double-layer film, as shown in Figure 1f. When we deposited a TiO_2 (VO_2) single layer, it functioned properly as a 1BR (1S) element (see Figure S1, Supporting Information). The resistance ratio between the ON and OFF states of the TiO_2 layer induces the sneak path problem if crossbar architecture is developed using only the 1BR single layer (see Figure S2, Supporting Information). Figure 1g shows the experimentally measured I–V characteristics of the TiO_2/VO_2 double layer. Note that this I–V curve is similar to that of the desired 1S-1BR device, as shown in Figure 1e.

To fabricate real 1S-1BR crossbar memory, we made 2 × 2 nanocrossbar arrays using the TiO_2/VO_2 films. **Figure 2**a shows a schematic of the nanocrossbar array device. The cross-sectional transmission electron microscopy (TEM) image shows that the TiO_2/VO_2 film was grown on a $Pt/SiO_2/Si$ substrate (Figure 2b). Figure 2c shows the top view of the 2 × 2 array of the device with a cell size of approximately 200 × 200 nm^2. Figure 2d shows the experimentally measured I–V characteristics of a cell in the nanocrossbar array. This curve is very similar to the ideal I–V curve of the 1S-1BR memory shown in Figure 1e. We confirm that the sneak path problem will not occur in this TiO_2/VO_2 nanocrossbar device; as shown in Figure 2e, the OFF state of cell #1 can be read correctly regardless of the states in all of the other cells. We also checked operations of the 1S-1BR device in the dc-sweep and the pulse modes (detailed operations are included in Figure S3a,b, Supporting Information). These operations demonstrated that the device functions satisfactorily as non-volatile memory without the sneak path problem.

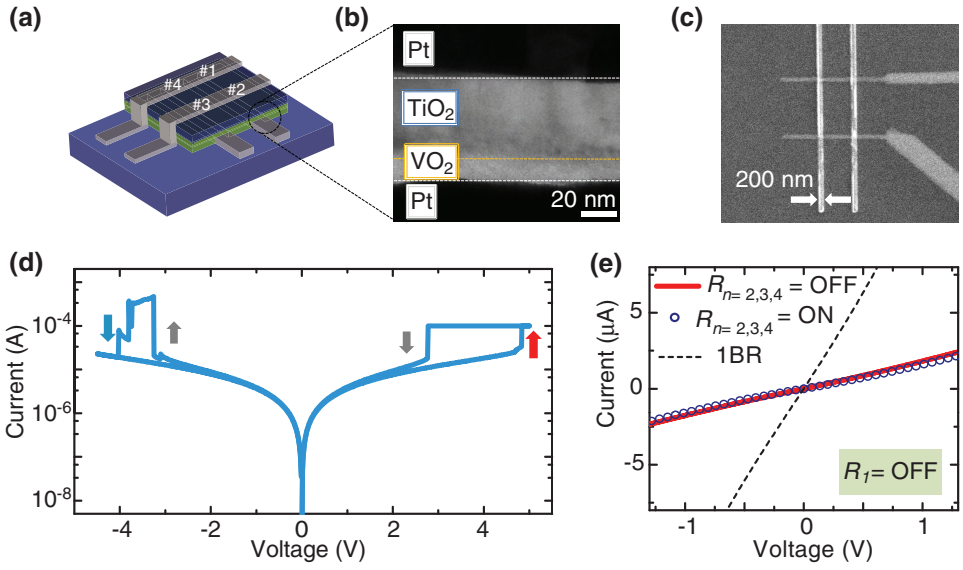

Figure 2. A 2 × 2 crossbar array TiO_2/VO_2 nanostructure and its electrical properties. a) A schematic of the 2 × 2 crossbar array for electrical measurements. b) A cross-sectional TEM image. c) A SEM image of the 2 × 2 crossbar array with an approximately 200 × 200 nm^2 sized, one-bit cell. d) The *I–V* curve of the TiO_2/VO_2 double layer in the 2 × 2 crossbar array. e) Confirmation of the absence of the sneak path problem in the 2 × 2 crossbar array.

The proposed 1S-1BR oxide nanocrossbar device architecture exhibits several advantages and possibilities for developing high-density memory. First, it is the simplest hybrid device structure that combines the functions of resistive memory and switching elements. Second, this simple patterned nanostructure does not contain an intermediate electrode, which has been commonly used in the previously proposed hybrid devices,[4–8] so it is easier to fabricate. Third, the cell size of the crossbar architecture is $4F^2$, which is the highest attainable density. Both 1S and 1BR elements can be reduced to smaller sizes without significantly affecting their performances. Note that the bipolar valence change memory effects, originate from oxygen vacancy migration in the TiO_2 cells, possess higher scalability potential compared to other types of resistive memory effects.[13] Fourth, the 2D double layer is easily stackable into a 3D crossbar architecture through its integration with n multilayers and using stackable peripheral circuits, which will further increase the scalability to provide an effective cell size of $4F^2/n$. Note that the peripheral circuits can control the compliance current in the crossbar architecture and help to operate properly. The use of an all-oxide-based structure makes the stacking and scaling down of peripheral circuits possible.[24] Finally, the switching elements in the crossbar array will reduce the leakage current significantly. If the $n \times n$ crossbar array is operated as shown in Figure 1a, the sources of the leakage current generally increase in proportion to n^2. However, in Figure 1b, $V_{read}/2$ and $-V_{read}/2$ are applied to the targeted word- and the bit-lines, respectively, and 0 V is applied to all of the other unselected lines. Because the nonzero voltage is applied only to the $2(n-1)$ cells sharing the word- or bit-lines, the source of the leakage current may increase linearly with n instead of n^2.

The ultimate scalability of this 1S-1BR device is determined by how small the oxide double layer device can be made without affecting its performance. Such lateral size limits, called the critical sizes, of TiO_2 as 1BR and VO_2 as 1S need to be further investigated in future. However, we can obtain an upper bound of the scalability limit by a simple test using conducting atomic force microscopy (C-AFM). As shown in **Figure 3**a, we tested the performance of the TiO_2/VO_2 double layer using a tip probe of the C-AFM as the top electrode. We used the solid Pt nanowire tip of the C-AFM from Park systems. The diameter of the tip was estimated to be about 10 nm using field-emission scanning electron microscopy (SEM; Hitachi SU-70). The inset of Figure 3a shows a schematic diagram of the C-AFM experimental setup with a 2.5 × 2.5 μm^2 current level mapping of the TiO_2/VO_2 double layer at 0.5 V. Initially, the pristine double layer sample exhibited highly insulating behavior. Figure 3a shows the experimental *I–V* curve of a local point in the TiO_2/VO_2 double layer by using dc-sweep mode. Note that the obtained *I–V* curve is similar to that of the nanocrossbar array shown in Figure 2d. Considering the size of the C-AFM tip, we can argue that the 2D TiO_2/VO_2 nanocrossbar memory should work with F = 10 nm, which corresponds to a density of 1.6 Tb $in.^{-2}$. Higher densities will be achievable if the nanocrossbar heterostructures are stacked in 3D.

Reset and leakage currents are very crucial limiting factors in real operations, since the power consumption will increase with a higher current level. Figure 3b shows how leakage and reset currents vary with changes in the cell size in the TiO_2/VO_2 double-layer device. These data were obtained from three different types of experiments using approximately 50 micrometer-sized top electrodes (brown circle in Figure 3b), the nanocrossbar structure with submicrometer widths (green), and the C-AFM (blue). As shown by the dashed guideline, the leakage current decreases approximately with the square of the cell size, i.e., area-dependence phenomena. And the reset current also shows a marked decrease with decreasing cell size and reaches below 10^{-8} A when it was measured with C-AFM. The reset current level is much lower than those of most other types of memory, which are typically higher than 10^{-5} A per cell.[27] And this value

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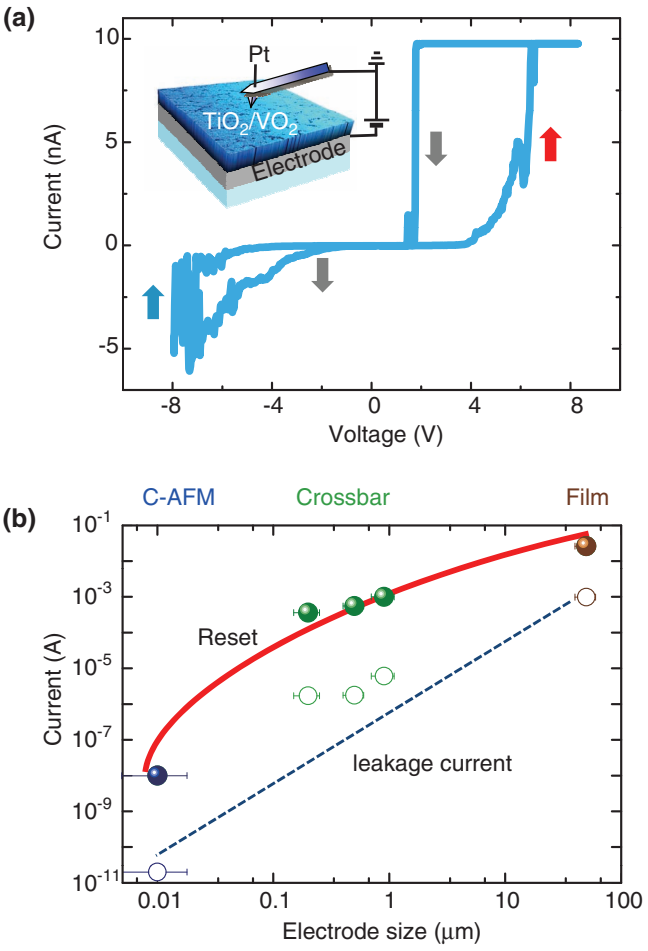

Figure 3. a) The experimentally measured local *I–V* curve, measured using C-AFM. The inset shows the schematic diagram of the C-AFM experimental setup. b) Scaling of the leakage and reset currents as a function of the cell dimension. The scaling behavior of levels of the current of the OFF state at 0.5 V and the reset current with the decrease of the electrode size from tens of micrometers to tens of nanometers in the TiO_2/VO_2 double-layer samples. The solid and open circles represent the reset current and leakage current, respectively. The solid line and the dotted line represent the guidelines for the reset current and the leakage current, respectively.

becomes comparable to the reported value of single Co_3O_4 nanowire with a diameter of about 10 nm, when it is used in bipolar resistive memory.[28] This work demonstrates that the 1S-1BR nanodevice could reduce the power consumption significantly with the decrease of the device size.

In summary, we have proposed a simple oxide double-layer nanocrossbar memory as a method of achieving ultrahigh-density memory. This hybrid memory combines a bipolar resistive memory and a bidirectional switch without an interlayer electrode. As a demonstration of such 1S-1BR device, a nanocrossbar array was fabricated using a TiO_2/VO_2 double layer. The 1S-1BR hybrid memory can work properly without the sneak path problem. The scaling behavior of the TiO_2/VO_2 memory cell from 50 μm to 10 nm was checked and very satisfactory results were obtained. Therefore, the 1S-1BR hybrid memory is promising as non-volatile memory with high-density and low power consumption.

Experimental Section

Thin Film Growth: Both polycrystalline TiO_2 and VO_2 layers (10–200 nm thick) were deposited at 600 °C, 5×10^{-6} Torr and 600 °C, 1.5×10^{-2} Torr, respectively, on a $Pt/TiO_x/SiO_2/Si$ substrate using a pulsed laser deposition (PLD) system. TiO_2/VO_2 heterostructure films, which exhibit polycrystallinity, were grown on a $Pt/TiO_x/SiO_2/Si$ substrate in the PLD system. A metallic $SrRuO_3$ film (20 nm thick) was grown on the films as a buffer layer before the deposition of the heterostructure film. The cell size of the 1BR, 1S, and 1S-1BR devices was approximately 50×50 μm^2.

Fabrication of the Crossbar Array: The Pt electrode was grown on a SiO_2/Si substrate through on-axis sputtering and electron beam lithography. The TiO_2/VO_2 heterostructure films were deposited without the $SrRuO_3$ buffer layer. The line-width of the top and bottom Pt electrodes was 200–1000 nm. TEM measurements were performed with a 200-kV field-emission TEM (Tecnai F20). The TEM specimens were prepared using a focused ion beam (FIB) etching technique.

Electric Measurements: *I–V* measurements were performed at room temperature using a semiconductor parameter analyzer (Agilent 4155C, Agilent Technologies). To prevent total dielectric breakdown, the current was limited to a maximum value called the compliance current. Pulse measurements were performed at room temperature using a YOKOGAWA FG300 synthesized function generator and a YOKOGAWA DL7100 digital oscilloscope. For the local *I–V* measurements, current amplification of C-AFM (XE-100, Park systems) was used with an external gain of 10^9 V A^{-1} to limit the current to the compliance current. To check the reproducibility of the local *I–V* measurements, both a solid Pt nanowire tip (customized by Park systems) and a Pt/Ir-coated tip (ANSCM-PT from Applied NanoStructure, Inc.) were used as C-AFM tips.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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